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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,766	10/29/2003	Akira Yamanoue	032069	5286

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/694,766	Applicant(s) YAMANOUE ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *12-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1-7, 9 and 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US Pat. 6452274) in view of Matsunaga et al. (US Pat. 6559548) and Hagiwara (see IDS; Japanese Pat. Pub. 2001168093).

Regarding claims 1-7, 9 and 10, Hasegawa et al. disclose a semiconductor device comprising:

- a first composite insulating/dielectric film layer/FCIL (see 64/68 in Fig. 7F) comprising a lower level insulating layer (LLIL) and lower dielectric layer (LDL) formed over semiconductor substrate (62 in Fig. 7F)
- a second composite insulating/dielectric film layer/SCIL (see 73/78 in Fig. 7F) comprising a second dielectric layer (SDL) and a third dielectric layer (TDL) formed over the FCIL
- the insulating/dielectric films being formed of a variety of polymer films including organosilicate glass, inorganic doped glass, etc. (see Col. 3, 4 and 20)

- an interconnection structure buried the FCIL and SCIL (see 66/71/76/81 in Fig. 7F), the interconnection structure being in a form of a pad (see 81 in Fig. 7F, 28 in Fig. 2I, etc.)
- a first dummy pattern of a first conducting layer such as copper (see 72 in Fig. 7F; Col. 20, line 30) buried in at least a surface side of the FCIL near the interconnection structure
- a second dummy pattern formed of a second conducting layer such as copper (see 82 in Fig. 7F; Col. 21, lines 13-15) buried the SCIL near interconnection structure and connected to the first dummy pattern through a via portion/groove shaped pattern (see 77 in Fig. 7B-7F), and
- the interconnection structure further including a first interconnection pattern (see 71 in the FCIL in Fig. 7F) formed of the first conductive layer/copper buried in the FCIL and a second interconnection pattern (see 81 in the SCIL in Fig. 7F; Col. 21, line 15) formed of the second conductive layer/copper buried in the SCIL and connected to the first interconnection pattern through a via portion/groove shaped pattern (see 76 in Fig. 7F)

(Fig. 7F; Col. 20, line 1- Col. 21, line 46).

Hasegawa et al. disclose the interconnection structure being buried in the first and second composite insulating films but fail to:

a) explicitly teach the same in the first and second insulating films, and

b) the first and second dummy patterns comprising a plurality of discrete patterns periodically formed so as to make a pattern density of the second conducting layer respectively substantially uniform in plane.

a) Matsunaga et al. teach a conventional interconnect structure (see Fig. 7E) comprising conductive wiring/pattern having vias and plugs (see 76/75 in Fig. 7E) where the interconnect structure is formed in a single insulating film (see 76/75 in the insulating film 74 in Fig. 7E; Col. 8, line 48- Col. 9, line 45). Furthermore, Matsunaga et al. teach using various insulating films being made of different material including a phospho-silicate glass, organosilicate glass (OSG), silicon oxide, etc. to achieve the desired dielectric properties and modulus (see 71, 74, 80, etc. in Fig. 7E; Col. 8, line 65- Col. 9, line 16).

b) Hagiwara teach a prior art multilayered wiring structure (see Fig. 6) having a dummy wiring comprising a plurality of discrete patterns including first and second dummy patterns (see 32 and 36 in Fig. 6). Hagiwara further teach a multilayered wiring structure (Fig. 1 and 2) having a second dummy wiring including a plurality of discrete patterns (see 8 in Fig. 1 and 2) being periodically formed in respective section/portion having conducting layer/plane so as to make a pattern density of the upper

conducting layer substantially uniform in the respective sections/portions of the plane (see 8 having high/low density in respective sections having the dummy wiring in Fig. 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a) and b) as taught by Matsunaga et al. and Hagiwara so that number of insulating layers can be reduced and photo/etch processing can be simplified in Hasegawa et al's device.

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US Pat. 6452274) and Matsunaga et al. (US Pat. 6559548) and Hagiwara (see IDS; Japanese Pat. Pub. 2001168093) as applied to claims 1 and 7 above and further in view of Shaffer, II et al. (US Pat. 2002/0052125).

Regarding claim 8, Hasegawa et al, Matsunaga et al. and Hagiwara teach substantially the entire claimed structure as applied to claims 1 and 7 above, including the insulating film being mainly formed of OSG, but fail to teach the first and the second insulating film being mainly formed of a polyallyl ether resin and organosilicate glass (OSG) respectively.

Shaffer, II et al. teach using an organic dielectric insulating material in an interconnect structure where the organic material comprises a number of polymers

including an organosilicate resin and polyarylene ether resin wherein functional /substitutional groups include a variety of groups including alkyl, alkenyl, alkylene, allyl,

aryl alkoxy, etc. to achieve the desired dielectric properties, adhesion and etching characteristics (see sections 0037-0042).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first and the second insulating film being mainly formed of a polyallyl ether resin and organosilicate glass (OSG) respectively as taught by Shaffer, II et al. so that the desired dielectric properties, adhesion and etching characteristics can be achieved in Hagiwara, Matsunaga et al. and Hasegawa et al's device.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US Pat. 6452274) in view of Matsunaga et al. (US Pat. 6559548).

Regarding claim 11, Hasegawa et al. disclose a semiconductor device having an insulating structure including a plurality of insulating layers (see Fig. 7F), the device comprising:

- a first composite insulating/dielectric film layer/FCIL (see 64/68 in Fig. 7F) comprising a lower level insulating layer (LLIL) and lower dielectric layer (LDL) formed over semiconductor substrate (62 in Fig. 7F)

- a second composite insulating/dielectric film layer/SCIL (see 73/78 in Fig. 7F) comprising a second dielectric layer (SDL) and a third dielectric layer (TDL) formed over the FCIL
- the insulating/dielectric films being formed of a variety of polymer films including organosilicate glass, inorganic doped glass, etc. (see Col. 3, 4 and 20)
- an interconnection structure buried the FCIL and SCIL (see 66/71/76/81 in Fig. 7F), the interconnection structure being in a form of a pad (see 81 in Fig. 7F, 28 in Fig. 2I, etc.)
- a first dummy pattern of a first conducting layer such as copper (see 72 in Fig. 7F; Col. 20, line 30) buried in at least a surface side of the FCIL near the interconnection structure
- a second dummy pattern formed of a second conducting layer such as copper (see 82 in Fig. 7F; Col. 21, lines 13-15) buried the SCIL near interconnection structure and connected to the first dummy pattern through a via portion/groove shaped pattern (see 77 in Fig. 7B-7F), and
- the interconnection structure further including a first interconnection pattern (see 71 in the FCIL in Fig. 7F) formed of the first conductive layer/copper buried in the FCIL and a second interconnection pattern (see 81 in the SCIL in Fig. 7F; Col. 21, line 15) formed of the second conductive layer/copper buried in the SCIL and connected to the first interconnection pattern through a via portion/groove shaped pattern (see 76 in Fig. 7F)

(Fig. 7F; Col. 20, line 1- Col. 21, line 46).

Hasegawa et al. disclose a plurality of dummy patterns but fail to explicitly teach the same in the respective insulating films.

Matsunaga et al. teach a conventional interconnect structure (see Fig. 7E) comprising conductive wiring/pattern having vias and plugs (see 76/75 in Fig. 7E) where the interconnect structure is formed in a single insulating film (see 76/75 in the insulating film 74 in Fig. 7E; Col. 8, line 48- Col. 9, line 45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of dummy patterns but fail to explicitly teach the same in the respective insulating films as taught by Matsunaga et al. and Hagiwara so that number of insulating layers can be reduced and processing can be simplified in Hasegawa et al's device.

Response to Arguments

5. Applicant's arguments filed on 02-28-05 have been fully considered but they are not persuasive.

A. Applicant contends that the dummy patterns of Hasegawa et al. differ from those of the invention since they are provided for the heat dispersion and not for reducing intra-plane variations of a polishing amount in the CMP process.

However, the limitations as recited in claims 1-11 do not include such features.

B. Applicant contends that the dummy patterns of Hagiwara are formed only in the peripheral regions and not in the whole region/major part of the chip.

However, the limitations as recited in claims 1-11 include the dummy patterns being near to interconnection structure, but do not include those being in the major part of the chip.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

04-25-04

NITIN PAREKH

PRIMARY EXAMINER

Technology Center 2800